IN THE CLAIMS

1-35. (Previously Cancelled)

36-55. (Canceled)

56. (New) A system providing peripheral component device interconnection, comprising:

a peripheral device processor for controlling operation of the peripheral device; and

a host messaging unit, coupled to the peripheral device processor, but separate from the peripheral device processor, the host messaging unit retrieving host commands from a host memory of a discrete host without adding process loading to the peripheral device processor, validating the retrieved host command and asynchronously signaling a successful transfer of the host commands from host memory to the host messaging unit.

57. (New) The system of claim 56, wherein the host messaging unit retrieves host commands from a host memory of a discrete host without adding process loading to a host processor of the discrete host.

58. (New) The system of claim 56, wherein the host messaging unit provides signaling between the peripheral device and the discrete host asynchronous to operation of the discrete host and the peripheral device.

59. (New) The system of claim 56, wherein the host messaging unit is disposed external to the peripheral device and provides signaling between a plurality of peripheral devices and the discrete host, the operation of the host messaging unit being asynchronous to operation of the discrete host and the peripheral devices.

60. (New) The system of claim 56, wherein the host messaging unit comprises:

a read controller, coupled to the bus, for determining when the host commands have been provided to the host memory and for retrieving the host commands directly from the host memory via direct memory access asynchronous to the operation of the host processor and the peripheral device;

a write controller, coupled to the bus and to the read controller, the write controller clearing the host memory to allow the host to infer that the host command has been read by the host messaging unit;

a validator, coupled to the write controller and the read controller, the validator determining a validity of host commands retrieved from the host memory;

a read clock, coupled to the read controller, the read clock providing a signal for initiating reading of host commands from the host memory by the read controller; and

a busmaster command engine, coupled to the validator, read controller and bus, the busmaster command engine initiating the command retrieval from the host memory when the busmaster command engine receives a signal from the discrete host indicating host commands are available in the host memory.

61. (New) The system of claim 60, wherein the busmaster command engine comprises a register programmable for indicating that the command is available to be retrieved from the host memory.

62. (New) The system of claim 60, wherein the read clock is programmable to allow predetermined retrieval intervals.

63. (New) The system of claim 60, wherein the read clock restarts the predetermined interval after the host commands are retrieved from the host memory.

64. (New) The system of claim 56, wherein the peripheral device processor further comprises a peripheral device means, operatively coupled via a bus means to host memory means, the peripheral device means including peripheral device processing for controlling operation of the peripheral device means and wherein the host messaging unit further comprises host messaging means, coupled to the peripheral device processing means, but separate from the peripheral device processing means, the host messaging means retrieving the host commands from host memory means of a discrete host means without adding process loading to the host processing means or the peripheral device processing means, validating the retrieved host command and asynchronously signaling a successful transfer of the host commands from host memory means to the host messaging means.

65. (New) A method of servicing a peripheral component interconnect device, comprising:

providing a host messaging unit operatively disposed between a discrete host having a host processor and a peripheral device processor for providing a signal interface that operates asynchronously with respect to the operation of the host processor and a the peripheral device;

receiving at the host messaging unit a signal indicating that the host processor has loaded a host command into host memory coupled to the host processor;

retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the peripheral device processor;

validating the retrieved host command at the host messaging unit; and

clearing the host memory to allow the discrete host to infer that the host command has been read by the host messaging unit; and

providing the host command to the peripheral device processor for processing by the peripheral device processor.

66. (New) The method of claim 64 further comprising retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the host processor of the discrete host.

67. (New) The method of claim 64, wherein the retrieving the host command directly from the host memory further comprises providing a clock to control the initiation of the retrieval of the host command from the host memory at predetermined intervals.

68. (New) An article of manufacture comprising:

a program storage medium readable by a computer, the medium tangibly embodying one or more programs of instructions executable by the computer to perform operations for reducing bus transfer overhead between a host processor and a peripheral component interconnect device processor, the operations comprising:

providing a host messaging unit operatively disposed between a discrete host having a host processor and a peripheral device processor for providing a signal interface that operates asynchronously with respect to the operation of the host processor and a the peripheral device;

receiving at the host messaging unit a signal indicating that the host processor has loaded a host command into host memory coupled to the host processor;

retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the peripheral device processor;

validating the retrieved host command at the host messaging unit; and

clearing the host memory to allow the discrete host to infer that the host command has been read by the host messaging unit; and

providing the host command to the peripheral device processor for processing by the peripheral device processor.